REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-11 are pending in the present application with Claims 1, 2, 4 and 9 having been amended by the present amendment

In the outstanding Office Action, Claims 1-3, 5-9 and 11 were rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al. in view of Delonibus and Abiko; Claim 4 was rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al. in view of Delonibus, Abiko and Misra et al.; and Claim 10 was rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al. in view of Delonibus, Abiko and Gardner et al.

Claims 1-3, 5-9 and 11 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Boyd et al. in view of Delonibus and Abiko. This rejection is respectfully traversed.

Claim 1 has been amended to recite that the method for fabricating an electronic component with a self-aligned source, drain and gate, includes the steps of forming a metal layer on the source, drain and dummy gate; superficial, self-aligned siliciding of the source and drain by selectively siliciding the metal layer on the source and the drain; and depositing at least one contact metal layer having a total thickness greater than the height of the dummy gate, polishing the at least one contact metal layer stopping at the dummy gate, and imparting an insulation characteristic to a surface region of the at least one contact metal layer and the metal layer on sides of the gate electrode.

In a non-limiting example, Figure 3 illustrates forming a metal layer 124 on the source, drain and dummy gate, and superficial, self-aligned siliciding of the source and drain by selectively siliciding the metal layer 124 and the source drain (see the regions 126 and 128). That is, the siliciding is selective insofar as it is limited to the zones in which the metal of the layer 124 is directly in contact with silicon. It can be seen in Figure 3 that the metal

layer 124 is disappeared above the source and drain regions to form superficial layers of silicide 126, 128. On the other hand, the metal layer 124 persists on the top sides of the dummy gate 112. On these parts, the silicon nitride of the layers 106 and 116 of the dummy gate and spacers has prevented siliciding (see page 10, line 27 to page 11, line 3).

Further, Figure 4 illustrates depositing at least one contact metal layer 130, 132, and Figure 6 illustrates imparting an insulation characteristic to a surface region of the at least one contact metal layer 130, 132 and the metal layer 124 on the sides of the gate electrode. That is, Figure 6 shows a step of imparting an insulating nature to the materials flush with the upper surface 136. During this step, oxidation is performed by subjecting the structure to an oxidizing atmosphere. To facilitate the reading of Figure 6, the oxidized parts are marked with the same references as the corresponding non-oxidized parts but are followed by the letter "a." The oxidized parts 124a, 130a and 132a are therefore respectively the oxidized superficial parts of the metal preserved on the sides of the gate, and initially used for siliciding the first contact metal and the second contact metal. The oxidation imparts an electrical insulating nature to the metals (see page 12, lines 11-25). The surface insulation is used as a stopping layer during planarization and as a protecting layer of the source and the drain regions.

The outstanding Office Action recognizes Boyd and Delonibus do not teach or suggest a surface insulation and relies on Abiko as teaching this feature and cites Figures 7A to 7G and column 3, lines 35-41. However, Applicant notes the cited portion in column 3, lines 35-41 does not correspond to the features shown in Figures 7A to 7G, but rather corresponds to features shown in Figure 4A, for example, in which a silicon nitride film 19 (i.e., a sealant) is formed over a silicide film 18 such that the silicide film 18 is not exposed to an atmosphere of the oxidation even when the silicide film 18 is exposed to a high temperature with the result that the deterioration of the silicide 18 can be prevented. Figures

7A-7G merely describe using a sealing portion 67 formed on a conductive film 66 (see column 6, lines 49-56). There is no discussion in Abiko for using the sealing portion 67 to prevent the exposure of the contact metal layer to an atmosphere that may oxidize the contact metal layer which may result in deterioration of the device (note this is referring to the sealing film 19 over the silicon nitride film 18 in Figure 4A). Thus, Applicant submits there would be no motivation to combine the references. Further, Applicant also notes that the sealing portion 67 in Abiko do not affect a metal layer formed on sides of the gate electrode 62. That is, the sides of the gate electrode 62 in Abiko (see Figure 7E, for example) are not imparted with an insulation characteristic. This differs from the claimed invention.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Further, regarding the additional rejections of the dependent claims noted in the outstanding Office Action, it is respectfully noted the additional publications of Misra et al. and Gardner et al. also do not teach or suggest the features recited in amended Claim1. Accordingly, it is respectfully request these rejections also be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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